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(54) SEMICONDUCTOR SURFACE PROTECTING METHOD

VERFAHREN ZUM SCHÜTZEN EINER HALBLEITEROBERFLÄCHE

PROCEDE POUR PROTEGER LA SURFACE D'UN SEMICONDUCTEUR

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Description

Technical Field

[0001] The present invention relates to a semiconductor surface protecting method for protection of the circuit-containing sides of a semiconductor wafer during the process of back side grinding of the wafers. More specifically, the invention relates to a semiconductor surface protecting method which permits ultrathin back side grinding of semiconductor wafers, or which permits back side grinding of semiconductor wafers having high protrusions such as solder bumps on the circuit side.

Background

[0002] Thinning (also referred to herein as "grinding") of semiconductor wafers has conventionally been accomplished by "back side grinding" methods whereby the circuit side of a wafer is protected with a surface protecting sheet and the back side opposite the circuit side is ground. The thicknesses of silicon wafers are generally 150 μm on an industrial level, but even thinner wafer thicknesses are desired. When wafers are ground to even smaller thicknesses, the phenomenon of unevenness of the ground surface (back side) due to irregularities on the circuit side, i.e., the phenomenon of transfer of the circuit pattern to the back side, becomes more notable. The cause of this back side transfer phenomenon is explained as follows. Presently employed pressure sensitive adhesive surface protecting sheets are limited in their ability to conform to the irregularities of the circuitry on a semiconductor wafer. As a result, gaps (air pockets) are created between the pressure-sensitive adhesive layer and the circuit side, such that the wafer is not directly supported by the pressure-sensitive adhesive (protective layer) in those areas. When the wafer is ground very thin, the wafer shifts in the vertical direction at the unsupported scribe lines (street) between the circuit die while compressing the air pockets with the result that the wafer is not ground in these areas, and remains thicker than the other portions. On the other hand, when hard protrusions such as bumps are present, the wafer is ground to a greater degree and thus becomes thinner than the other portions. This phenomenon is not a problem if the finished thickness is 150 μm or greater, but if the wafer is thinned to less than 100 μm (especially when finishing to a thickness of 50 μm or less), or if tall protrusions such as bumps are present on the wafer circuit side (for example, at 100 μm or greater), not only is the transverse strength of the wafer reduced considerably, but in severe cases the wafer can even be damaged during grinding. Also, when a wafer is thinly ground to about 50 μm, edge chipping of the wafer or penetration of grinding water between the wafer and surface protecting layer can constitute a problem, but this has also been caused by a lack of adhesion of the surface protecting sheet to the wafer edges. In addition, with semiconductor wafers which are thin and also have bumps or other protrusions of 100 μm or greater on the circuit side, it is difficult to accomplish grinding by attachment of typical surface protecting sheets.

[0003] A conventional surface protecting sheet is usually a sheet having a pressure-sensitive adhesive layer as a surface protecting layer on a polymeric film material. The pressure-sensitive adhesive is designed so as to have a low elastic modulus in order to follow irregularities on the circuit side. If this tendency is too strong, however, the wafer can undergo considerable stress and suffer damage when the sheet is removed by peeling from the wafer. This has led to the development of energy beam peelable protecting sheets wherein the pressure-sensitive adhesive is hardened by irradiation with an energy beam such as ultraviolet rays to lower the adhesive strength between the wafer and protecting sheet before peeling. However, an often occurring problem is that the pressure-sensitive adhesive layer is too flexible in the unhardened state during grinding, and the wafer thus suffers damage during grinding.

[0004] Japanese Unexamined Patent Publication HEI No. 11-26404 discloses a wafer grinding method whereby the aforementioned energy beam peelable protecting sheet is attached to a circuit-formed wafer and the pressure-sensitive adhesive layer is hardened with an energy beam, after which the back side of the wafer is ground. However, since the pressure-sensitive adhesive is not fluid, its conformability against irregularities on the wafer circuit side is not adequate.

[0005] Japanese Unexamined Patent Publication No. 2000-38556 and EP-A-0 977 254 disclose a hot-melt semiconductor surface protecting sheet. The hot-melt sheet melts and exhibits fluid properties by heating at 60-100°C, and thus is able to conform to irregularities on the circuit side and exhibit excellent grinding properties. However, the sheet repeatedly melts when the temperature rises above the melting point. In most cases, a semiconductor wafer which has been laminated with a protective sheet is subjected to subsequent heating during lamination of a film used for attachment of chips, or a "die attachment film" (hereinafter referred to as "DAF"), or during a metal film forming step by sputtering. As a result, the temperature increase produced in such steps has caused problems including remelting of the protective sheet.

Summary of the Invention

[0006] It is an object of one aspect of the present invention to provide a semiconductor surface protecting method

employing a material having an adequate conformability for irregularities on a semiconductor wafer circuit side and sufficient rigidity as a support during grinding, and which does not become fluid with repeated temperature increase, as well as a surface protecting sheet which can be used in the method.

[0007] Generally, the invention provides a semiconductor surface protecting method whereby the circuit side of a semiconductor wafer is protected during the process of back side grinding of the wafer, said method comprising joining the circuit side of the semiconductor wafer to a polymeric film material by means of a fluid surface protecting layer which hardens upon radiation exposure or heating, and hardening the surface protecting layer.

[0008] According to one mode, the invention provides a semiconductor surface protecting method whereby the circuit side of a semiconductor wafer is protected during the process of back side grinding of the wafer, the method comprising joining the circuit side of the semiconductor wafer to a polymeric film material via a surface protecting layer which is either fluid at room temperature or may be made so by heating and which hardens upon radiation exposure or heating, and hardening the surface protecting layer.

[0009] According to another mode, the invention provides a semiconductor surface protecting method whereby the circuit side of a semiconductor wafer is protected during back side grinding of the wafer, the method comprising providing a surface protecting sheet comprising a polymeric film material on which is formed a surface protecting layer which is solid at room temperature, becomes fluid upon heating and hardens upon exposure to radiation or upon heating to a temperature higher than the fluidizing temperature, heating said surface protecting sheet to render the surface protecting layer fluid, placing the circuit side of said semiconductor wafer in contact with the fluidized surface protecting layer, and hardening the surface protecting layer.

[0010] According to yet another mode, the invention provides the use of a surface protecting sheet for protection of the circuit side of a semiconductor wafer during back side grinding of the wafer, the surface protecting sheet comprising a polymeric film material on which is provided a surface protecting layer which is solid at room temperature, becomes fluid upon heating and hardens upon exposure to radiation or upon heating to a temperature higher than the fluidizing temperature.

[0011] In the aforementioned methods, the surface protecting layer contacts the wafer circuit side while in a fluid state and therefore a sufficient conformability is provided for the surface profile formed on the circuit side. The protecting layer having sufficient conformability exhibits high rigidity when hardened, and thus protects the wafer circuit side. Also, once the protecting layer is hardened, it does not refluidize during subsequent heating steps such as a die attachment film laminating step or sputtering metal film formation step.

[0012] The aforementioned protecting methods may be carried out using the aforementioned surface protecting sheet.

[0013] Throughout the present specification, the term "fluid" refers to the state of the viscoelastic profile of a sample wherein the elastic shear loss modulus (G") is greater than the elastic shear storage modulus (G'), or Tanδ (= G"/G') is greater than, or equal to, one.

[0014] Throughout the present specification, the terms "elastic shear storage modulus (G')" and "elastic shear loss modulus (G")" refer, respectively, to the elastic shear storage modulus and elastic shear loss modulus of the surface protecting layer material before hardening. The shear storage and loss moduli values are recorded on a chart using a viscoelasticity measuring apparatus at a frequency of 10 Hz, a deformation of 0.04% and a temperature-ramp rate of 3°C/min.

[0015] More specifically, they were measured using a viscoelasticity measuring apparatus (ARES, product of Rheometrics), for test samples of the surface protecting layers having a diameter of 25 mm and a thickness of 0.6 mm.

[0016] The terms "elastic tensile storage modulus (E')" and "elastic tensile loss modulus (E")" refer, respectively, to the elastic tensile storage modulus and elastic tensile loss modulus after hardening. The tensile storage and loss moduli values are recorded on a chart using a viscoelasticity measuring apparatus at a frequency of 1 Hz, a deformation of 0.04% and a temperature-ramp rate of 5°C/min.

[0017] More specifically, they were measured using a viscoelasticity measuring apparatus (SOLIDS ANALYZER RSA II, product of Rheometrics), for test samples of the surface protecting layers cut to 22.7 mm × 10 mm × 50 μm, after hardening (for example, after ultraviolet irradiation for 3 seconds with an 80 W/cm high-pressure mercury lamp).

[0018] The invention will now be explained in greater detail with reference to the accompanying drawings.

[0019] Figure 1 is a first flow chart for one embodiment of the semiconductor surface protecting method of the invention.

[0020] First, a fluid surface protecting layer material which can be hardened by light or heat is provided (Step (a)). The material of the surface protecting layer may be a liquid at room temperature (about 20-25°C) or a solid at room temperature which is fluidized by heating. The surface protecting layer 3 material is then evenly coated on the circuit side 2 of a wafer 1 (Step (b)). A polymeric film material 4 is then placed over the protecting layer 3 (Step (c)), and the protecting layer 3 is hardened by ultraviolet rays or heating (Step (d)). During this procedure, care must be taken to avoid inclusion of air at the interface between the protecting layer 3 and the wafer 1, the interface between the protecting layer 3 and the polymeric film material 4, or in the protecting layer 3. Inclusion of air will prevent a smooth grinding surface on the wafer, making it impossible to thinly grind the wafer to an even thickness, or possibly leading to damage of the wafer during grinding. Conducting the procedure in a vacuum can prevent air inclusion.

[0021] Figure 2 is a second flow chart for another embodiment of the semiconductor surface protecting method of the invention.

[0022] First, a surface protecting layer 3, which is a solid at room temperature (about 20-25°C) and which can be hardened by light irradiation or heating at high temperature is formed on a polymeric film material 4 to prepare a surface protecting sheet 5 (Step (a)). This may be done using solution coating and drying methods or by hot melt coating methods. Next, the surface protecting sheet 5 is heated at a sufficient temperature for fluidization of the protecting layer 3 (Step (b)). The wafer 1 is placed over the fluidized protecting layer so that the circuit side 2 is in contact with the protecting layer 3 (Step (c)). A solid is formed again upon cooling of the protecting layer 3 (Step (c')). Reforming the solid will facilitate handling of the wafer/protecting sheet laminate. The protecting layer 3 may then hardened by ultraviolet rays or heat. If heat is employed, then the temperature used is greater that that required for fluidization of the surface protecting layer (Step (d)). This series of steps may also be carried out in a vacuum for the same reasons as in the first flow chart. However, it was found more convenient to conduct the heating of Step (b) and the contact of Step (c) using a heating laminator. When a heating laminator is used, inclusion of air can be prevented by gradually contacting the wafer 1 with the heat-fluidized protecting layer 3 from the edge of the wafer.

Brief Description of the Drawings

[0023]

Fig. 1 is a first flow chart for a semiconductor surface protecting method of one embodiment of the invention.
Fig. 2 is a second flow chart for a semiconductor surface protecting method of another embodiment of the invention.

Detailed Description

[0024] A surface protecting sheet as used in the invention will now be explained.

Surface Protecting Layer

[0025] In one embodiment the surface protecting layer of the surface protecting sheet as used in the invention is a material which is solid at room temperature, becomes fluid upon heating and hardens upon exposure to radiation or upon heating to a temperature higher than the fluidizing temperature. As mentioned above, the term "fluid" refers to the state of the viscoelastic profile of a sample wherein the elastic shear loss modulus (G") is greater than the elastic shear storage modulus (G'), or Tanδ (= G"/G') $\geq$ 1. The fluidizing temperature of the solid surface protecting layer is preferably 30-100°C and more preferably about 35-60°C. If the temperature at which Tanδ = 1 is above 100°C, the procedure must be conducted at above 100°C for lamination of the surface protecting sheet, which is disadvantageous in terms of equipment and productivity. If the temperature at which Tanδ = 1 is below 30°C, and especially below room temperature (20°C), the storage stability will be poor when the sheet is wrapped into a roll and stored. The hardened protecting layer preferably has an elastic tensile storage modulus (E') of 5×10^7 Pa or greater at 50°C. This level of elastic modulus can ensure adequate rigidity as a support during grinding, and permit grinding of wafers to extremely thin and uniform thicknesses.

[0026] In another embodiment, the surface protecting layer is a fluid at room temperature and hardens upon exposure to radiation or upon heating to a temperature higher than room temperature.

[0027] Preferably, the surface protecting layer contains a polymerizable compound having two or more ethylenically unsaturated moieties or two or more cationically polymerizable groups in the molecule. As specific materials for the surface protecting layer which contain two or more ethylenically unsaturated moieties there may be mentioned free-radical polymerizable compounds such as (1) low molecular compounds which are crystalline or waxy at room temperature (20- 5°C), including isocyanuric acid-derived (meth)acrylates such as trisacryloxyethyl isocyanurate or trismethacryloxyethyl isocyanurate, pentaerythritol-derived (meth)acrylates such as pentaerythritol tetramethacrylate or pentaerythritol diacrylate monostearate, or bisphenol A-derived (meth)acrylates such as bisphenol A dimethacrylate; (2) urethane (meth)acrylate resins of molecular weight 10,000 or greater which are solid at room temperature; or (3) the following resins having a molecular weight of 1000 or greater which are solid at room temperature (20-25°C): phenol-novolac epoxy (meth)acrylate resins, cresol-novolac epoxy (meth)acrylate resins and bisphenol A epoxy di(meth)acrylate resins.

[0028] As specific materials for the surface protecting layer there may also be suitably used cationic polymerizable compounds including 1) epoxy-based low molecular compounds such as hydroquinone diglycidyl ether or diglycidyl terephthalate, which are crystalline or waxy at room temperature; and 2) phenol-novolac epoxy resins, cresol-novolac epoxy resins and bisphenol A epoxy resins of molecular weight 1000 or greater which are solid at room temperature.

[0029] In another embodiment, the surface protecting layer is a fluid at room temperature and hardens upon exposure to radiation and/or upon heating to a temperature higher than room temperature. The material for the surface protecting

layer may also contain a polymerizable compound which is liquid at ordinary temperatures, so long as the layer can be handled as a solid at ordinary temperatures after addition of each component. As examples of liquid free-radical polymerizable compounds there may be mentioned (meth)acrylate compounds such as trimethylolpropane tri(meth)acrylate, pentaerythritol tri(meth)acrylate, pentaerythritol tetra(meth)acrylate, dipentaerythritol monohydroxypenta(meth)acrylate, dipentaerythritol hexa(meth)acrylate and 1,6-hexanediol di(meth)acrylate, or vinyl ether derivatives such as ethyleneglycol divinyl ether.

[0030] As liquid cationically polymerizable compounds there may be mentioned a polyepoxide containing compounds such as sorbitol tetraglycidyl ether, pentaerythritol tetraglycidyl ether, trimethylolpropane triglycidyl ether and bisphenol A diglycidyl ether, and the like.

[0031] The surface protecting layer may further contain a thermoplastic resin having a melting point or softening point in a range of 25-100°C together with the polymerizable compound, in an amount which does not impede the object of the invention. Representative examples of thermoplastic resins include polyolefin copolymers such as low density polyethylene (LDPE), ethylene-ethyl acrylate copolymer (EEA), ethylenevinyl acetate copolymer (EVA) and ionomer resins (IONO), thermoplastic elastomers such as butadiene-based elastomers, styrene-isoprene based elastomers and ester-based elastomers, acrylic resins such as methyl methacrylate, polyvinyl chloride-based resins such as vinyl chloride-vinyl acetate copolymer, thermoplastic polyesters, polyurethane, and the like. These are used for the purpose of raising or adjusting the fluidizing temperature ($Tan\delta \geq 1$) of the surface protecting layer before hardening. They can also confer flexibility to the protecting layer after hardening.

[0032] When the surface protecting layer is a photosetting or photocurable type which is hardened by exposure to radiation, it will usually include a photoinitiator which absorbs light to produce free-radicals or cations in order to initiate the polymerization reaction. As specific free-radical polymerization initiators there may be mentioned benzoin, benzoin methyl ether, benzoin ethyl ether, benzoin isopropyl ether, benzyldiphenyl sulfide, azobisisobutyronitrile, dibenzyl, diacetyl, acetophenone, diethoxyacetophenone, 1-hydroxycyclohexylphenyl ketone, 2-hydroxy-2-methyl-1-phenylpropan-1-one and 2-benzyl-2-dimethylamino-1-(4-morpholinophenyl)-butanone-1, and as specific cationic polymerization initiators there may be mentioned allyldiazonium salts, allylsulfonium salts, allyliodonium salts and the like. The amount of the free radical polymerization initiator or cationic polymerization initiator is not particularly restricted, but will normally be 0.1-10 wt% based on the weight of the polymerizable compound.

[0033] For thermosetting types that are hardened by heating, the protecting layer will generally include a thermopolymerization initiator. Thermopolymerization initiators include azobisisobutyronitrile, benzoyl peroxide and the like.

[0034] The surface protecting layer may also contain an additive such as a filler, antioxidant, plasticizer or the like, in a range that does not impair the desired properties such as fluidity and post-hardening elastic tensile storage modules. The thickness of the surface protecting layer may be set as desired within a range of at least 10 μm greater than magnitude of the surface profile on the circuit-containing side of the semiconductor wafer, but considering uniformity of the total thickness of the surface protection sheet as a whole, it is generally 20-300 μm (inclusive), preferably 30-200 μm and more preferably 50-150 μm.

Polymeric Film Material

[0035] In one embodiment the polymeric film material supports the surface protecting layer to provide a sheet. The polymeric film material is not particularly restricted so long as it is a polymer film with a uniform thickness suitable for this use. However, when exposure to radiation such as ultraviolet rays or visible light rays is used to harden the surface protecting layer, it must be adequately permeable to ultraviolet rays (or visible light). For example, there may be used polyesters such as polyethylene terephthalate, polyolefin resins such as polypropylene, or polyvinyl chloride resins, polyvinylidene chloride resins, polyamide resins and the like. The thickness of the film is not particularly restricted, but is preferably such as to provide bending flexibility suitable for peeling removal of the film together with the protecting layer from the circuitized side of the wafer. The polymeric film material will therefore usually be 50-300 μm in thickness.

Manufacturing Method

[0036] In one embodiment the surface protecting sheet is manufactured in the following manner. A solid material forming the surface protecting layer is heated (at about 50-100°C, for example) to fluidize it. The fluid layer is then evenly coated onto a suitable polymeric film material such as a polyester film using appropriate means, such as a knife coater, and then allowed to cool to form a surface protecting sheet according to the invention. Alternatively, the solid material of the protecting layer may be dissolved in an appropriate solvent such as methyl ethyl ketone (MEK) to prepare a coating solution, and this solution may then be evenly coated onto a polymeric film material in the same manner and the solvent evaporated off to obtain a surface protecting sheet according to the invention.

Method of Using a Surface Protecting Sheet

[0037] In one embodiment the surface protecting sheet as used in the invention may be laminated by contact bonding to the circuit side of a semiconductor wafer either after heating or during heating. The sheet and circuit side of the wafer may also be contact bonded in a vacuum chamber. Such methods can accomplish complete lamination without inclusion of air bubbles.

[0038] The side opposite the circuit side of the wafer is ground to thin the wafer, with the circuit side protected by the surface protecting sheet. The ground surface is then processed by a polishing step. As polishing steps there may be mentioned chemical etching, chemical mechanical polishing (CMP), dry polishing or the like, which are commonly used for this purpose. Depending on the application, this may be followed by any desired metal film formation step such as sputtering or vapor deposition, or a step of laminating a die attachment film necessary for mounting of a chip. Although these steps are heating steps, the surface protecting sheet of the invention has adequate heat resistance and can therefore tolerate such steps. The wafer obtained by the aforementioned back side treatment steps is then attached by lamination of the ground and polished side to a dicing sheet, after which the surface protecting sheet is removed by peeling it off before the subsequent dicing step.

[0039] The above explanation assumes a semiconductor surface protecting method employing a surface protecting sheet, but as shown in the flow chart of Fig. 1, the method of the invention may also be carried out using a fluid protecting layer. The material for the protecting layer in this case may be the same material as used for the aforementioned protecting sheet, but it may also be a material which is fluid at room temperature. Consequently, there may be used free-radical polymerizable compounds which are liquid at room temperature, for example, trimethylolpropane tri(meth)acrylate, pentaerythritol tri(meth)acrylate, pentaerythritol tetra(meth)acrylate, dipentaerythritol monohydroxypenta(meth)acrylate, dipentaerythritol hexa(meth)acrylate and 1,6-hexanediol di(meth)acrylate, or vinyl ether derivatives such as ethyleneglycol divinyl ether, and cationically polymerizable compounds which are liquid at room temperature, for example, polyepoxide compounds such as sorbitol tetraglycidyl ether, pentaerythritol tetraglycidyl ether, trimethylolpropane triglycidyl ether and bisphenol A diglycidyl ether, and the like. The aforementioned thermoplastic resins may also be included.

[0040] The surface protecting sheet of the invention is not limited to protection of the circuit side of a semiconductor wafer, and may instead be effectively applied for other uses requiring a conformability to surface irregularities.

Examples

1. Protecting layer composition for surface protecting sheet, and manufacture and testing of protecting sheets

[0041] Mixtures having the following compositions were used as materials for protecting layers of surface protecting sheets. The compositions for Examples 1-3 and the Comparative Example were solid at room temperature. The composition for Example 4 was liquid at room temperature.

1.1. Protecting layer composition

Example 1 (Ultraviolet curing solid protecting layer)

[0042]

Table 1

Chemical Name	Product Name	Weight Percent
Urethane acrylate	UV3520TL	76.1%
Tris(acryloxyethyl) isocyanurate	M315	19.1%
2-Benzyl-2-dimethylamino-1-(4-morpholinophenyl)-butanone-1	Irgacure 369	4.8%
		100.0%

Example 2 (Ultraviolet curing solid protecting layer)

[0043]

Table 2

Chemical Name	Product Name	Weight Percent
Urethane acrylate	UV3510TL	76.2%
Bisphenol A diacrylate	VR90	19.0%
2-Benzyl-2-dimethylamino-1-(4-morpholinophenyl)-butanone-1	Irgacure 369	4.8%
		100.0%

Example 3 (Ultraviolet curing solid protecting layer)

[0044]

Table 3

Chemical Name	Product Name	Weight Percent
Urethane acrylate	UV3510TL	57.1%
Bisphenol A diacrylate	VR90	38.1%
2-Benzyl-2-dimethylamino-1-(4-morpholinophenyl)-butanone-1	Irgacure 369	4.8%
		100.0%

Example 4 (Ultraviolet curing liquid protecting layer)

[0045]

Table 4

Chemical Name	Product Name	Weight Percent
Urethane acrylate	UV6100B	57.1%
1,6-Hexanedioldiacrylate	1,6-HX-A	38.1%
2-Benzyl-2-dimethylamino-1-(4-morpholinophenyl)-butanone-1	Irgacure 369	4.8%
		100.0%

Comparative Example (thermoplastic surface protecting layer)

[0046] "pbw" means parts by weight

Table 5

Chemical Name	Product Name	Weight Percent
Reaction product of 100 pbw of a copolymer of butyl acrylate:2-hydroxyethyl acrylate (70:30 w/w) and 30 pbw methacryloyloxy ethyl isocyanate	-	98.5%
Trifunctional isocyanate derived from toluene diisocyanate and 2-ethyl-2-(hydroxymethyl)-1,3-propanediol	Coronate L	0.5%
2-Benzyl-2-dimethylamino-1-(4-morpholinophenyl)-butanone-1	Irgacure 369	1.0%
		100.0%

UV3510TL (Nippon Synthetic Chemical Industry Co., Ltd.)
UV3520TL (Nippon Synthetic Chemical Industry Co., Ltd.)
1,6-HX-A (KYOEISHA CHEMICAL CO., LTD)
VR90 (SHOWA HIGHPOLYMER CO., LTD)
M315 (Toa Gosei Kagaku Co., Ltd.)

Irgacure 369 (Ciba Specialty Chemicals)
Coronate L (Nippon Polyurethane Industry Co., Ltd.)

1.2. Manufacture of surface protecting sheet

A) Solid (at room temperature) Surface Protection Layer

[0047] A 70% solids by weight solution of each of the surface protecting layer composition in MEK (methyl ethyl ketone) was prepared using the compositions of Examples 1-3 and the Comparative Example. These solutions were then knife coated onto 100 μm thick polyethylene terephthalate (PET) films and dried in an oven at 100°C to provide surface protecting sheets having a surface protecting layer thickness of about 50 μm.

B) Liquid (at room temperature) Surface Protection Layer

[0048] The composition of Example 4, which had a room temperature viscosity of 100 centipoise when measured at a shear rate of 1.86 sec^{-1}, was spin-coated onto a semiconductor wafer.
[0049] The resulting surface protecting layer had a thickness of about 50 μm.

1.3. Lamination

A) Solid (at room temperature) Surface Protection Layer

[0050] The surface protecting sheets of the examples were each taped at their edges to a glass plate which was held to the bottom face of a vacuum chamber such that the surface protecting layer was exposed, then heated to 70°C with hot air to fluidize the surface protecting layer to a highly viscous liquid state. Next, the vacuum chamber was lowered down over a silicon wafer having its circuit pattern side facing upward and then the chamber was evacuated prior to releasing the glass plate with the protection sheet/fluidized surface protecting layer taped thereto, and contacting it to the circuitized side of the wafer. The vacuum chamber was removed and the glass plate was detached from the surface protecting sheet/semiconductor wafer article. The protecting layer was then hardened by exposure to ultraviolet rays from the polymeric film material side. This was done using a Fusion UV lamp ("Light Hammier" LH6, available from Fusion UV Systems Inc., Gaithersburg, Maryland) which provided a UV intensity distribution on an 8 inch semiconductor wafer as follows: about 240 milliWatts/cm^2 at the center point of the wafer and about 150 milliWatts/cm^2 at the edge of the wafer. The exposure time was 3 seconds.
[0051] The surface protecting sheet of the Comparative Example was fluidized and laminated onto the circuit pattern side of a silicon wafer at a temperature of about 60°C using a hand roller.

B) Liquid (at room temperature) Surface Protection Layer

[0052] A glass plate having a polyester film taped thereto was secured to the bottom of a vacuum chamber. Next, the vacuum chamber was lowered down over a silicon wafer whose circuitized, upward facing surface was covered with a liquid surface protecting layer coating. The chamber was then evacuated prior to releasing the glass plate with the polyester film taped thereto, and contacting the film to the liquid surface protecting layer on the wafer. The combination of the polyester film and liquid surface protecting layer formed a surface protection sheet on the wafer. The vacuum chamber was removed and the glass plate was detached from the surface protection sheet/semiconductor wafer article. The protecting layer was then hardened by exposure to ultraviolet rays from the polymeric film material side as described in Section A above.

1.4. Back side grinding

[0053]. The silicon wafers protected on the circuit pattern sides with the surface protecting sheets of the Examples and Comparative Example were subjected to back side grinding to a 50 μm finish.

1.5. Heat resistance test

[0054] The silicon wafers protected on the circuit pattern sides with the surface protecting sheets of the Examples and Comparative Example were ground to a 50 μm thickness. The ground wafers, having the surface protection sheets thereon, were then placed on a 180°C hot plate with the surface protecting sheet in contact with the hot plate and kept there for 3 minutes.

1.6. Confirmation of conformability property

[0055] The protecting sheet was removed by hand at a peeling angle of 180 degrees from the silicon wafer, and the protecting layer surface profile and wafer circuit side surface profile were measured using a contact roughness meter.

1.7. Viscoelastic measurements

[0056] The elastic shear storage modulus (G') and elastic shear loss modulus (G") were measured using a viscoelastic measuring apparatus (ARES, available from Rheometrics) at a frequency of 10 Hz, a deformation of 0.04% and a temperature-ramp rate of 3°C/min. in temperature-ramp mode. The test samples of the unhardened surface protecting layers measured 25 mm in diameter and 0.6 mm in thickness. The elastic tensile storage modulus (E') and elastic tensile loss modulus (E") were measured using a viscoelastic measuring apparatus (SOLIDS ANALYZER RSA II, available from Rheometrics) at a frequency of 1 Hz, a deformation of 0.04% and a temperature-ramp rate of 5°C/min in temperature-ramp mode. The test samples of the hardened surface protecting layers measured 22.7 mm by 10 mm by 50 μm.

2. Test results

2.1. Results of viscoelasticity profile measurement

[0057]

Table 6

		Example 1	Example 2	Example 3	Example 4
Before hardening	Temperature at which Shear tanδ = 1	35°C	45°C	43°C	N.A.
After hardening	50°C elastic tensile storage modulus (E')	9×10^8 (Pa)	5×10^7 (Pa)	3×10^8 (Pa)	8×10^7 (Pa)

2.2. Back side grinding

[0058] When the wafers protected with the protecting sheets of Examples 1-4 were subjected to back side grinding down to a thickness of 50 μm, satisfactory grinding results were obtained with no circuit pattern back side transfer or edge chipping. In the Comparative Example, however, circuit pattern backside transfer was already visible at a ground thickness of 100 μm, and continued grinding produced edge chipping at about half the outer periphery of the wafer, at a thickness of 70 μm. Finally, grinding down to 50 μm resulted in penetration of grinding water from the edge sections, and caused damage in most of the wafer.

2.3. Heat resistance test

[0059] For Examples 1-4 no problems were observed in peeling the surface protection layer from the wafer. The Comparative Example was difficult to peel off.

2.4. Confirmation of conformability property

[0060] The surface profile of the circuit side of the semiconductor wafer matched that of the surface protecting layer surface that contacted the circuit side of the wafer in Examples 1-4. This confirmed the ability of the surface protecting layer to conform to the circuit side irregularities.

[0061] According to the present invention, the surface protecting layer exhibits a sufficient conformability for the irregularities on semiconductor wafer circuit surfaces and sufficient rigidity as a support during grinding, while also not being fluidized upon repeated temperature increases. Therefore, problems such as circuit pattern back side transfer or wafer damage do not occur even with back side grinding down to extremely low thicknesses of about 50 μm.

[0062] In one embodiment the surface protecting layer of a surface protecting sheet of the invention is solid at room temperature and can be provided as a sheet article, and since it is converted to a fluid liquid adhesive upon heating at 30-100°C, it may be laminated after heating to sufficiently conform to circuit side irregularities. Also, since in the fluid state the surface protecting layer wraps around the wafer edges by surface tension, the wafer is supported by the protecting layer even at the edges. Moreover, since the protecting layer is hardened into a high elastic modulus material by exposure to ultraviolet rays before grinding, it is possible to achieve excellent grinding properties (no back side transfer

of circuit side irregularities or wafer edge chipping, and no penetration of grinding water), similar to a system employing a liquid UV curing (or thermosetting) adhesive or wax for attachment of the wafer onto a hard substrate, such as by lamination. In other words, the protecting sheet of the invention achieves both the convenience of a sheet article and the excellent grinding properties of a process wherein the wafer is laminated onto a supporting substrate with a wax or liquid adhesive.

[0063] In another embodiment, the surface protecting layer may be provided as liquid at room temperature. Such a form permits coating directly onto an irregular surface followed by addition of a polymeric film to the liquid surface and subsequent hardening to provide a removable sheet article. This embodiment provides the same advantages as cited above.

Claims

1. A semiconductor surface protecting method whereby the circuit side of a semiconductor wafer is protected during the step of back side grinding of the wafer, comprising:

   joining the circuit side of said semiconductor wafer to a polymeric film material via a fluid surface protecting layer which hardens upon radiation exposure or heating, and
   hardening said surface protecting layer.

2. The method of claim 1, further comprising:

   providing a surface protecting sheet comprising a polymeric film material on which is said surface protecting layer which is solid at room temperature, becomes fluid upon heating and hardens upon exposure to radiation or upon heating to a temperature higher than the fluidizing temperature,
   heating said surface protecting sheet to make the surface protecting layer effectively fluid, and
   placing the circuit side of said semiconductor wafer in contact with the fluidized surface protecting layer, before the step of hardening said surface protecting layer.

3. Use of a surface protecting sheet for protection of the circuit side of a semiconductor wafer during the step of back side grinding of the wafer, the surface protecting sheet comprising a polymeric film material on which is formed a surface protecting layer which is solid at room temperature, becomes fluid upon heating and hardens upon exposure to radiation or upon heating to a temperature higher than the fluidizing temperature.

4. Use of a surface protecting sheet according to claim 3, wherein, before hardening of the surface protective layer, the protective layer has an elastic shear loss modulus (G") less than its elastic shear storage modulus (G') at room temperature (20-25°C) and an elastic shear loss modulus (G") greater than its elastic shear storage modulus (G') at 30-100°C, as measured with a viscoelasticity measuring apparatus at a frequency of 10 Hz, a deformation of 0.04% and a temperature ramp rate of 3°C/min., and the surface protective layer after hardening has an elastic tensile storage modulus (E') at 50°C greater than 5×10^7 Pa as measured with a viscoelasticity measuring apparatus at a frequency of 1 Hz, a deformation of 0.04% and a temperature-ramp rate of 5°C/min.

5. Use of a surface protecting sheet according to claim 3 or 4, wherein the surface protecting layer contains at least one type of a free-radical polymerizable compound having two or more ethylenically unsaturated moieties in the molecule, the free-radical polymerizable compounds being selected from the group consisting of:

   (1) (meth)acrylic-based low molecular weight compounds, selected from isocyanuric acid-derived (meth)acrylates, pentaerythritol-derived (meth)acrylates or bisphenol A-derived (meth)acrylates, which are crystalline or waxy at room temperature (20-25°C),
   (2) urethane (meth)acrylate resins of molecular weight 10,000 or greater which are solid at room temperature (20-25°C), and
   (3) the following resins having a molecular weight of 1000 or greater which are solid at room temperature (20-25°C): phenol-novolac epoxy (meth)acrylate resins, cresol-novolac epoxy (meth)acrylate resins and bisphenol A epoxy di(meth)acrylate resins.

6. Use of a surface protecting sheet according to claim 5, wherein the surface protecting layer further contains a free-radical polymerization initiator.

7. Use of a surface protecting sheet according to claim 3 or 4, wherein the surface protecting layer contains at least one cationically polymerizable compound having two or more cationically polymerizable groups in the molecule, the cationically polymerizable compounds being selected from the group consisting of:

   (1) epoxy-based low molecular compounds, selected from hydroquinone diglycidyl ether or diglycidyl terephthalate, which are crystalline or waxy at room temperature (20-25°C), and
   (2) phenol-novolac epoxy resins, cresol-novolac epoxy resins and bisphenol A epoxy resins of molecular weight 1000 or greater which are solid at room temperature.

8. Use of a surface protecting sheet according to claim 7, wherein the surface protecting layer further contains a cationic polymerization initiator.

Patentansprüche

1. Verfahren zum Schützen einer Halbleiteroberfläche, durch welches die Schaltungsseite eines Halbleiter-Wafers während des Schrittes des Schleifens der Rückseite des Wafers geschützt wird, wobei das Verfahren das Folgende aufweist:

   Verbinden der Schaltungsseite des Halbleiter-Wafers mit einem polymeren Filmmaterial über eine fließfähige Oberflächenschutzschicht, welche nach Bestrahlung oder Erwärmung härtet, und
   Härten der Oberflächenschutzschicht.

2. Verfahren nach Anspruch 1, welches ferner das Folgende aufweist:

   Bereitstellen einer Oberflächenschutzfolie, welche ein polymeres Filmmaterial aufweist, auf welchem sich die Oberflächenschutzs.chicht befindet, welche bei Raumtemperatur fest ist, nach Erwärmung fließfähig wird und nach Bestrahlung oder nach Erwärmung auf eine höhere Temperatur als die Fluidisierungstemperatur härtet,
   Erwärmen der Oberflächenschutzfolie, um die Oberflächenschutzschicht wirkungsvoll fließfähig zu machen, und .
   Inkontaktbringen der Schaltungsseite des Halbleiter-Wafers mit der fließfähig gemachten Oberflächenschutzschicht vor dem Schritt des Härtens der Oberflächenschutzschicht.

3. Verwendung einer Oberflächenschutzfolie zum Schützen der Schaltungsseite eines Halbleiter-Wafers während des Schrittes des Schleifens der Rückseite des Wafers, wobei die Oberflächenschutzfolie ein polymeres Filmmaterial aufweist, auf welchem eine Oberflächenschutzschicht gebildet ist, welche bei Raumtemperatur fest ist, nach Erwärmung fließfähig wird und nach Bestrahlung oder nach Erwärmung auf eine höhere Temperatur als die Fluidisierungstemperatur härtet.

4. Verwendung einer Oberflächenschutzfolie nach Anspruch 3, wobei vor der Härtung der Oberflächenschutzschicht die Schutzschicht einen elastischen Scher-Verlustmodul (G") aufweist, der geringer ist als ihr elastischer Scher-Speichermodul (G') bei Raumtemperatur .(20 bis 25 °C), und einen elastischen Scher-Verlustmodul (G") aufweist, der größer ist als ihr elastischer Scher-Speichermodul (G') bei 30 bis 100 °C, gemessen mit einer Viskoelastizitäts-Messvorrichtung bei einer Frequenz von 10 Hz, einer Verformung von 0,0.4 % und einer Temperatursteigerung von 3 °C/Min., und die Oberflächenschutzschicht nach der Härtung einen elastischen Zug-Speichermodul (E') bei 50 °C von mehr als 5 x 10^7 Pa aufweist, gemessen mit einer Viskoelastizitäts-Messvorrichtung bei einer Frequenz von 1 Hz, einer Verformung von 0,04 % und einer Temperatursteigerung von 5°C/Min.

5. Verwendung einer Oberflächenschutzfolie nach Anspruch 3 oder 4, wobei die Oberflächenschutzschicht mindestens einen Typ einer mit Hilfe freier Radikale polymerisierbaren Verbindung enthält, welche zwei oder mehr ethylenisch ungesättigte Einheiten im Molekül aufweist, wobei die mit Hilfe freier Radikale polymerisierbaren Verbindungen ausgewählt werden aus der Gruppe, bestehend aus:

   (1) Verbindungen niedrigen Molekulargewichts auf (Meth)acryl-Basis, ausgewählt aus (Meth)acrylaten, die aus Isocyanursäure abgeleitet sind, (Meth)acrylaten, die aus Pentaerythrit abgeleitet sind, und (Meth)acrylaten, die aus Bisphenol-A abgeleitet sind, welche bei Raumtemperatur (20 bis 25 °C) kristallin oder wachsartig sind,
   (2) Urethan(meth)acrylat-Harzen eines Molekulargewichts von 10.000 oder mehr, welche bei Raumtemperatur (20 bis 25 °C) fest sind, und

(3) den folgenden Harzen, welche ein Molekulargewicht von 1.000 oder mehr aufweisen und bei Raumtemperatur (20 bis 25. °C) fest sind: Phenol-Novolak-Epoxy(meth)acrylat-Harzen, Cresol-Novolak-Epoxy(meth)acrylat-Harzen und Bisphenol-A-Epoxydi(meth)acrylat-Harzen.

6. Verwendung einer Oberflächenschutzfolie nach Anspruch 5, wobei die Oberflächenschutzschicht ferner einen Initiator für die Polymerisation mit Hilfe freier Radikale enthält.

7. Verwendung einer Oberflächenschutzfolie nach Anspruch 3 oder 4, wobei die Oberflächenschutzschicht mindestens eine kationisch polymerisierbare Verbindung enthält, welche zwei oder mehr kationisch polymerisierbare Gruppen im Molekül aufweist, wobei die kationisch polymerisierbaren Verbindungen ausgewählt sind aus der Gruppe, bestehend aus:

(1) Verbindungen niedrigen Molekulargewichts auf Epoxybasis, ausgewählt aus Hydrochinondiglycidylether und Diglycidylterephthalat, welche bei Raumtemperatur (20 bis 25 °C) kristallin oder wachsartig sind, und
(2) Phenol-Novolak-Epoxidharzen, Cresol-Novolak-Epoxidharzen und Bisphenol-A-Epoxidharzen eines Molekulargewichts von 1.000 oder mehr, welche bei Raumtemperatur fest sind.

8. Verwendung einer Oberflächenschutzfolie nach Anspruch 7, wobei die Oberflächenschutzschicht ferner einen Initiator für die kationische Polymerisation enthält.

Revendications

1. Méthode de protection de la surface d'un semi-conducteur, par laquelle le côté circuit d'une tranche de semi-conducteur est protégé durant l'étape de meulage de l'envers de la tranche, comprenant :

l'assemblage du côté circuit de ladite tranche de semi-conducteur et d'un matériau sous forme de film polymère par l'intermédiaire d'une couche fluide de protection de surface qui durcit quand elle est exposée à un rayonnement ou chauffée, et
le durcissement de ladite couche de protection de surface.

2. Méthode selon la revendication 1, comprenant en outre :

la fourniture d'une feuille de protection de surface comprenant un matériau sous forme de film polymère sur lequel se trouve ladite couche de protection de surface qui est solide à la température ambiante, devient fluide quand elle est chauffée, et durcit quand elle est exposée à un rayonnement ou quand elle est chauffée à une température supérieure à la température de fluidisation,
le chauffage de ladite feuille de protection de surface pour rendre la couche de protection de surface effectivement fluide, et
le positionnement du côté circuit de ladite tranche de semi-conducteur en contact avec la couche de protection de surface fluidisée, avant l'étape de durcissement de ladite couche de protection de surface.

3. Utilisation d'une feuille de protection de surface pour la protection du côté circuit d'une tranche de semi-conducteur durant l'étape de meulage de l'envers de la tranche, la feuille de protection de surface comprenant un matériau sous forme de film polymère sur lequel est formée une couche de protection de surface qui est solide à la température ambiante, devient fluide quand elle est- chauffée, et durcit quand elle est exposée à un rayonnement ou quand elle est chauffée à une température supérieure à la température de fluidisation.

4. Utilisation d'une feuille de protection de surface selon la revendication 3, dans laquelle, avant le durcissement de la couche de protection de surface, la couche de protection a un module élastique de perte en cisaillement (G") inférieur à son module élastique de conservation en cisaillement (G') à la température ambiante (20-25 °C) et un module élastique de perte en cisaillement (G") supérieur à son module élastique de conservation en cisaillement (G') à 30-100 °C, mesurés avec un appareil de mesure de viscoélasticité à une fréquence de 10 Hz, une déformation de 0,04 % et une vitesse d'augmentation de la température de 3 °C/min, et la couche de protection de surface après le durcissement a un module élastique de conservation en traction (E') à 50 °C qui est supérieur à 5×10^7 Pa, mesuré avec un appareil de mesure de viscoélasticité à une fréquence de 1 Hz, une déformation de 0,04 % et une vitesse d'augmentation de la température de 5 °C/min.

5. Utilisation d'une feuille de protection de surface selon la revendication 3 ou 4, dans laquelle la couche de protection de surface contient au moins un type d'un composé polymérisable par radicaux libres comportant deux fractions à insaturation éthylénique ou plus dans la molécule, les composés polymérisables par radicaux libres étant sélectionnés dans le groupe constitué de:

(1) composés (méth)acryliques de faible masse moléculaire, sélectionnés parmi les (méth)acrylates dérivés d'acide isocyanurique, les (méth)acrylates dérivés de pentaérythritol ou les (méth)acrylates dérivés de bisphénol A, qui sont cristallins ou cireux à la température ambiante (20-25 °C)
(2) résines (méth)acrylate d'uréthane ayant une masse moléculaire de 10 000 ou plus, qui sont solides à la température ambiante (20-25 °C), et
(3) les résines suivantes ayant une masse moléculaire de 1 000 ou plus, qui sont solides à la température ambiante (20-25 °C) : résines (méth)acrylate époxy de type phénol-novolaque, résines (méth)acrylate époxy de type crésol-novolaque, et résines di(méth)acrylate époxy de bisphénol A.

6. Utilisation d'une feuille de protection de surface selon la revendication 5, dans laquelle la couche de protection de surface contient en outre un initiateur de polymérisation par radicaux libres.

7. Utilisation d'une feuille de protection de surface selon la revendication 3 ou 4, dans laquelle la couche de protection de surface contient au moins un composé polymérisable par polymérisation cationique comportant deux groupes polymérisables par polymérisation cationique ou plus dans la molécule, les composés polymérisables par polymérisation cationique étant sélectionnés dans le groupe constitué de:

(1) composés époxy à faible masse moléculaire, sélectionnés parmi l'éther diglycidylique d'hydroquinone ou le téréphtalate diglycidylique, qui sont cristallins ou cireux à la température ambiante ,(20-25 °C), et
(2) résines époxy de type phénol-novolaque, résines époxy de type crésol-novolaque, et résines époxy de bisphénol A ayant une masse moléculaire de 1 000 ou plus, qui sont solides à la température ambiante.

8. Utilisation d'une feuille de protection de surface selon la revendication 7, dans laquelle la couche de protection de surface contient en outre un initiateur de polymérisation cationique.

Fig. 1a

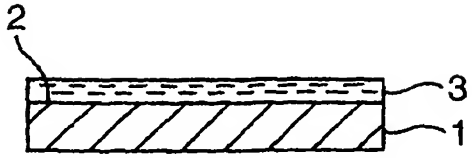

Fig. 1b

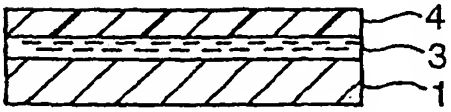

Fig. 1c

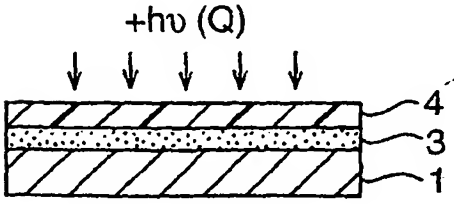

Fig. 1d

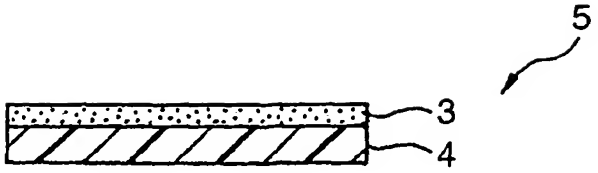

Fig. 2a

Fig. 2b

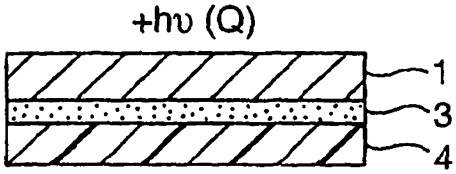

Fig. 2c

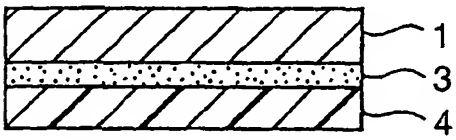

Fig. 2d

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

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- JP 2000038556 A **[0005]**
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